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Engineering Note

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Subject: How To Design With Orcad

Introduction

This note describes the process of designing a printed circuit board using Orcad Capture design tools. It is meant to augment and amplify the generic instruction given in the Orcad documentation to define a more restrictive set of rules to insure consistent designs. This is not an Orcad tutorial; for that, read the program documentation. It is, however, meant to teach better principles of design which can be utilized with all CAE programs. However, since we use Orcad, the examples are drawn from Orcad.

Basic Rules

1. All sheets within a schematic shall be the same page size. Use 'B' throughout if possible; if not, use 'C' or 'D' and reduce to fit 'B' size when printing. ANSI Y.14 rules shall be followed for all sheets.
2. If the schematic will not entirely fit within one sheet, the first sheet shall be a block diagram and the schematic shall be drawn as a simple hierarchy.
3. No complex hierarchies will be allowed. A complex hierarchy may be utilized during concept design but it must be reduced to a simple hierarchy prior to release to PCB layout.
4. Schematics shall be reviewed a minimum of twice prior to PCB layout; once during a concept review and once during a pre-layout review.
5. All schematics shall have a D0 document number, assigned after the concept review and prior to the pre-layout review. This document number shall appear on every page of the schematic.
6. On all pages, inputs shall be at the left and outputs shall be at the right. On all symbols, inputs shall be at the left and outputs shall be at the right except that individual "glue logic" gates may be rotated as necessary to show signal flow.
7. If a symbol for a component exists within an Orcad library, that symbol shall be used. New symbols which must be created shall be created in project-specific libraries. Upon release of a schematic to PCB layout, a copy of the project symbol library shall be archived on the D0 server for use by later projects.

Design Process

1. Enter the schematic using Capture.
   1.1. Use **Place Part** to get symbols from libraries.
   1.2. Connect symbols using wires and buses. Wires connect to buses using **Bus Entries.**
   1.3. Individual wires connected to buses must be individually labeled to insure connectivity. Buses have the name syntax **XXX[n..m];** a wire connected to that bus would be labeled **XXXn**. When using hierarchical blocks, insure that the names of signals entering and leaving the block (hierarchical pin names) are consistent with the internal and external signal names.

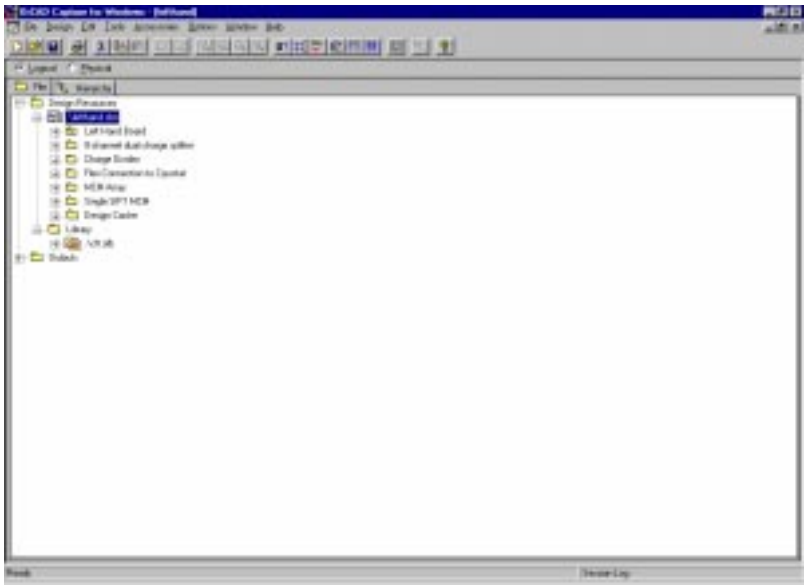
2. When the schematic is complete, use **Annotation** to insure that all parts in the schematic have unique reference designators.

   2.1. When a design is flat or a simple hierarchy, annotation works flawlessly. However, if a schematic is in the complex hierarchy form (e.g. multiple hierarchical blocks point to the same sub-sheet), **annotation** will not work unless the project is in the **physical** view mode. This is one reason not to use a complex hierarchy.

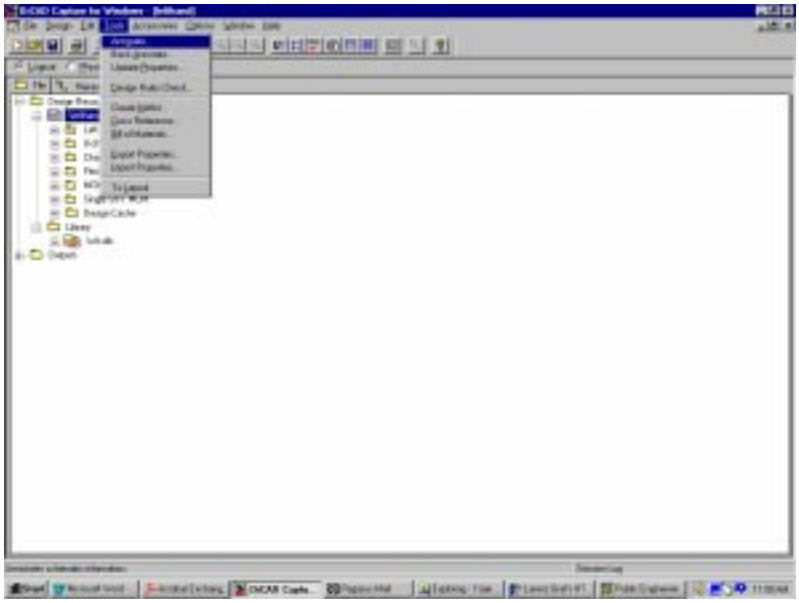
   2.2. A second problem with a complex hierarchy is that all instances of the sub-sheet must be identical. You can't make small changes between all the instances; all details are fixed. This can cause severe routing problems or introduce bad component placement.

   2.3. **Annotation** simply runs through the design and assigns a unique reference designator to all objects in the schematic. Make certain that you check the **unconditional annotation** box; do not use incremental annotation.

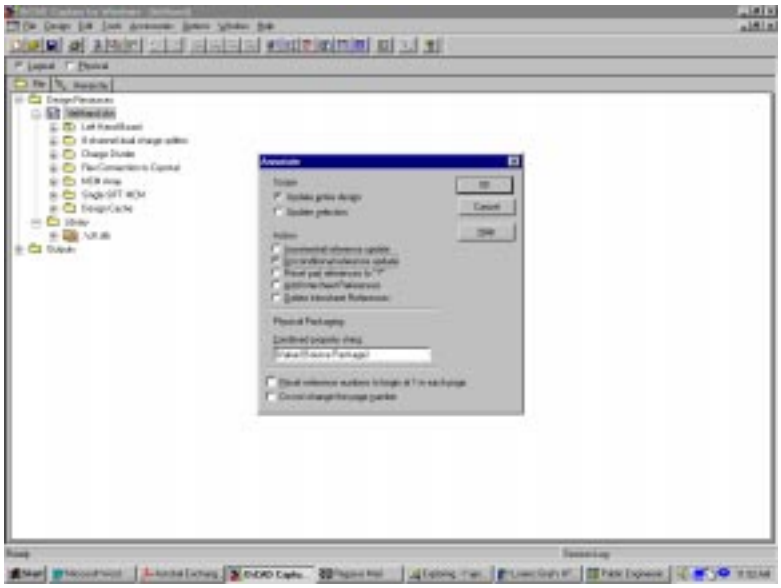
   2.4. The step by step procedure is simple. Select the root of the design in the project view window.



   2.5. Select **Tools..Annotate.**



   2.6. Select **Update Entire Design** and **Unconditional Reference Update.** Then hit **OK.**

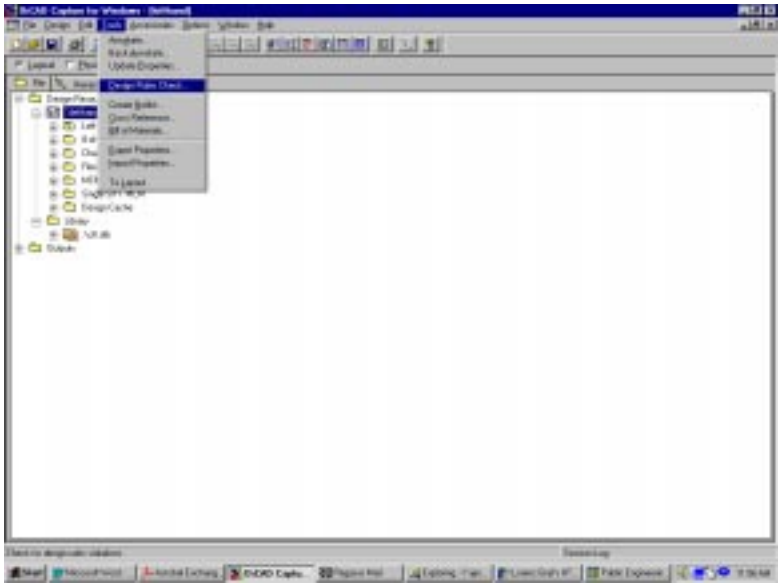


2.7. A log of annotation results is given in the **Session Log.** Insure no warnings or errors are generated.

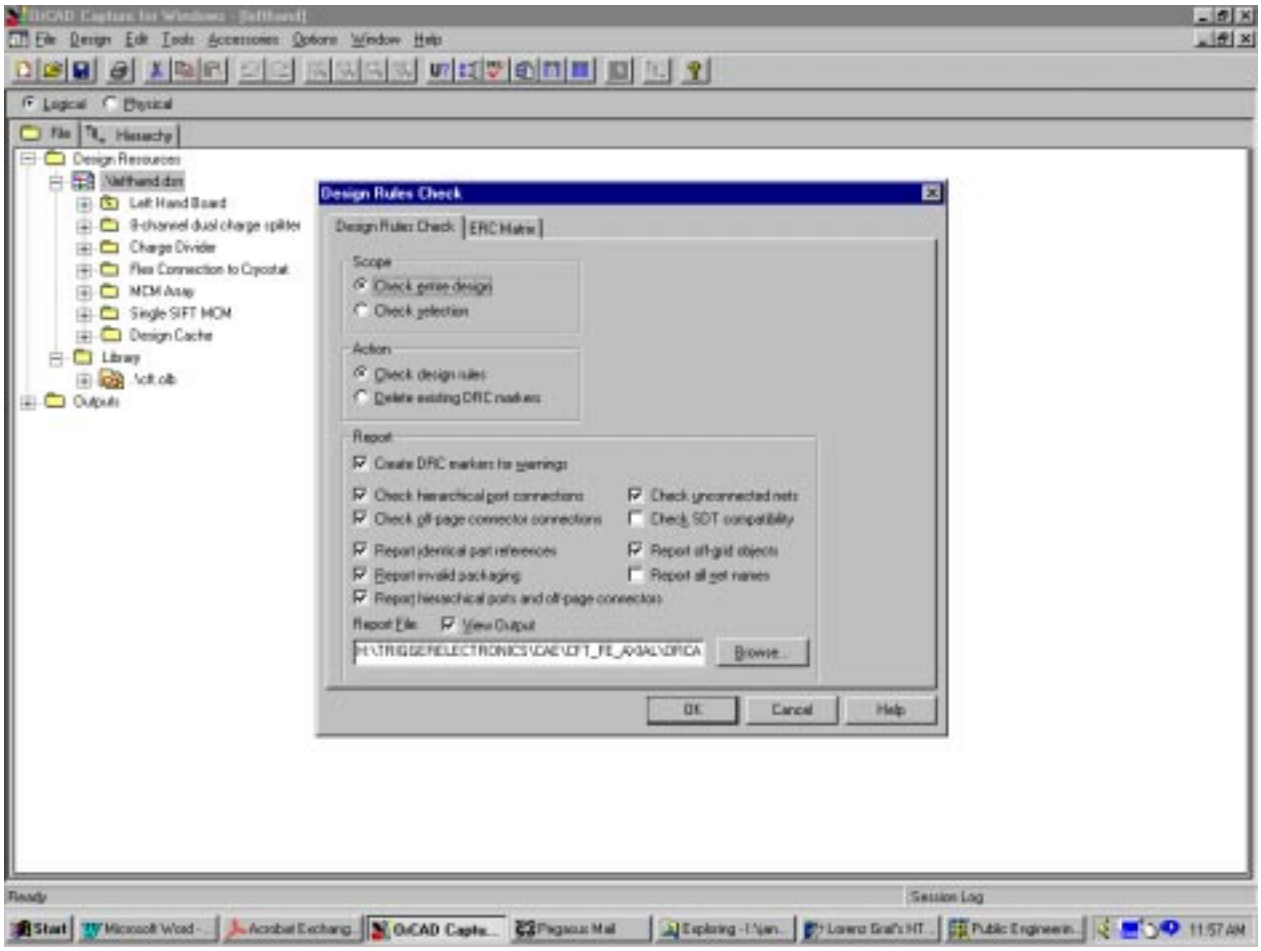
3. After the design has been annotated, the next step is to perform a **Design Rules Check**.

3.1. Again, make sure the root of the design is selected.

3.2. Then use the **Tools…Design Rule Check** menu selection.



3.3. Make certain the entire design is checked; also make use of the options to get better information. I usually use the set as shown here. Do *not* modify the ERC matrix. The default is correct for all designs. Hierarchical ports should always be checked to insure that blocks and the sheets they reference match.



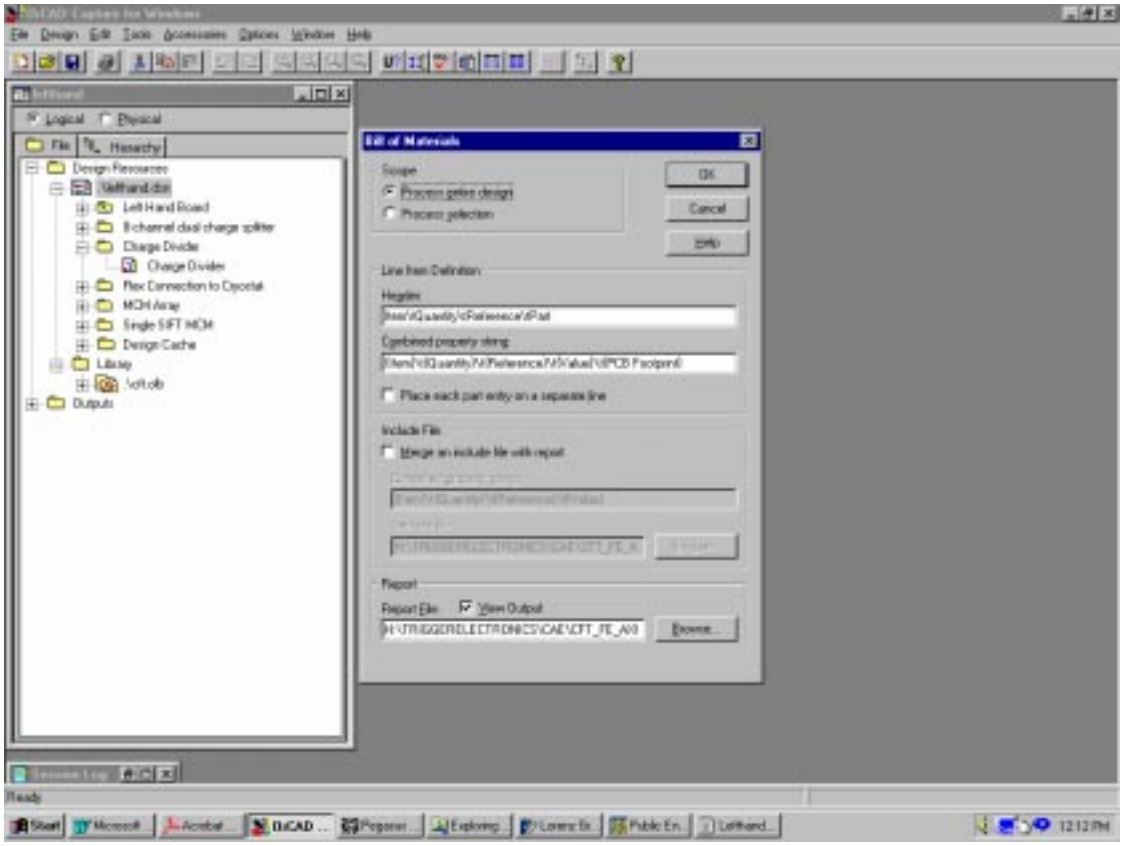
3.4. With the **View Output** box checked, the DRC file will be displayed. All errors *must* be corrected before one may proceed; *almost all* warnings need also be corrected. In rare instances a warning may be ignored:

3.4.1. In ECL designs where multiple outputs are intentionally shorted to create a wire-OR;

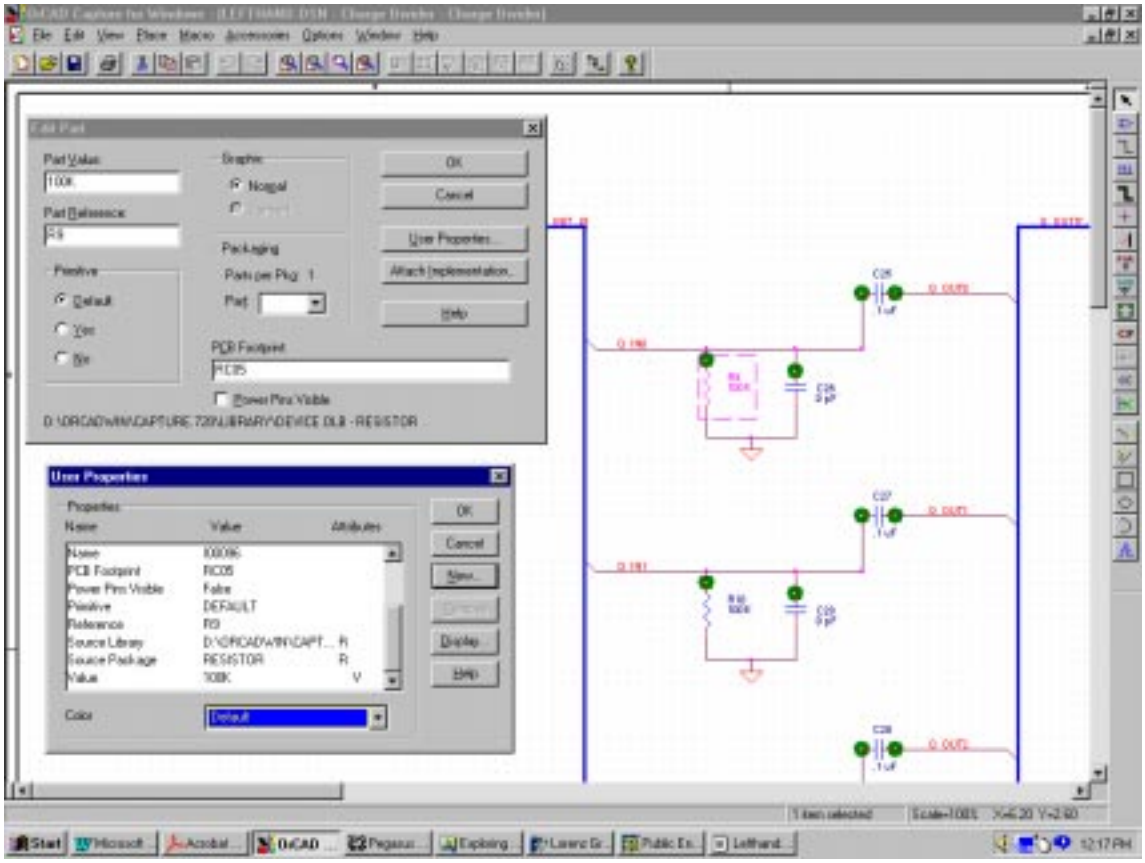
3.4.2. In field-programmable logic designs where unused pins are shorted to create 'green wire' buses for later logic changes.

3.5. Many DRC warnings and errors are created by incorrect pin type entries in user defined parts. Insure that pins which can be either input or output are correctly categorized; if unsure, use *passive*.

4. The next useful output is the **Bill of Materials**. The BOM gives a detailed list of every component in the design. Although usually considered a procurement step, generating the BOM is critical to insuring a clean transition to the PCB layout. Selecting the **Tools…Bill of Materials** menu selection yields the following dialog box:



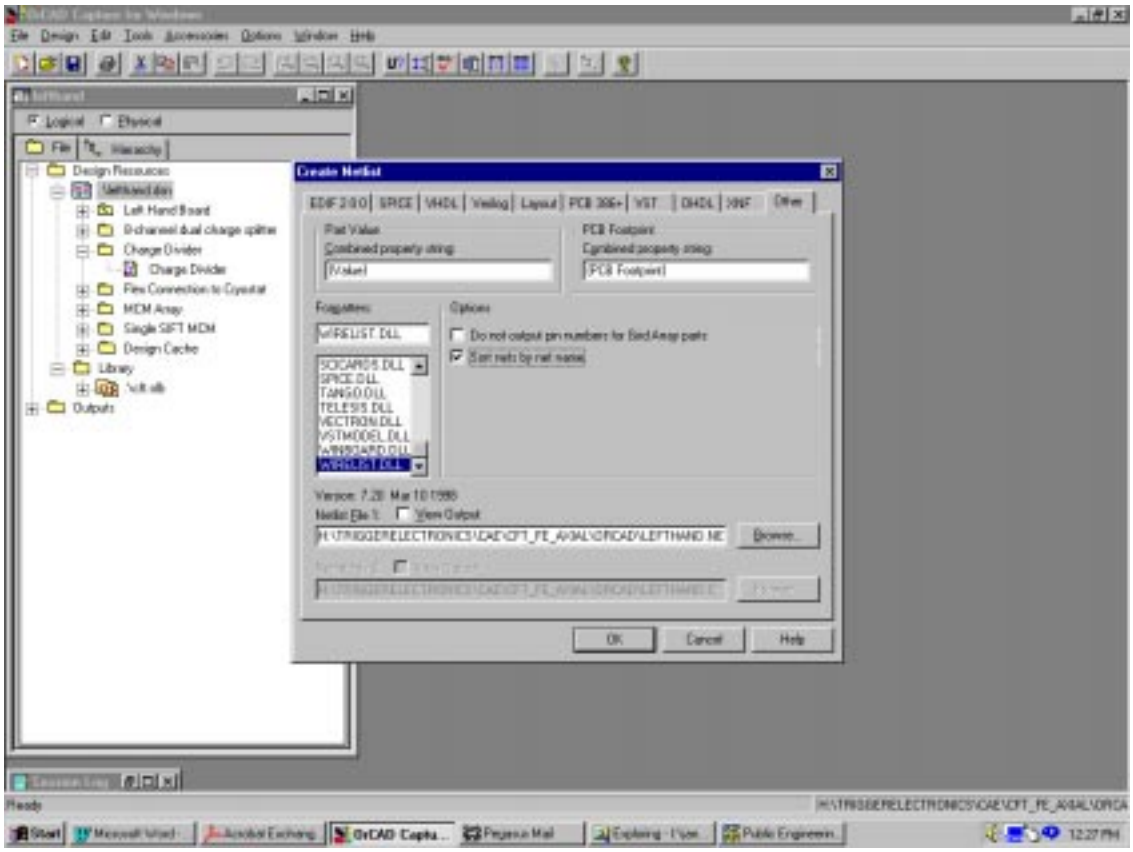
4.1. The critical entry here is the **Combined Property String**. Each item in curly braces is one of the properties of the component within the schematic. These properties are available when editing the schematic, as shown here:



4.2. Everything listed in the User Properties can be used as a field in the Bill of Materials. By default, the item number, part value and reference designator are printed; however, the PCB Footprint should also be included. The '\t' separators in the Bill of Materials indicate tab characters; this means that the Bill of Materials file is easily imported into spreadsheets to form orders. For small jobs, it is often useful to add new User Properties such as the Digi-Key part number as you enter the schematic; the Bill of Materials then will create all the ordering data you need.

4.3. Careful examination of the Bill of Materials with PCB Footprints added will often catch layout problems before layout occurs.

5. After the Bill of Materials is successfully generated, you're ready to use **Tools…To Layout**. The **Tools…Create Netlist** option is only used if the netlist has to be exported to something other than Layout for Windows. The option is useful for small wirewrap jobs; for this, select the **other** tab and use the WIRELIST.DLL format as shown.



6. When **Tools…Layout** is finished, archive everything (schematics, netlist, BOM, etc.) and hand it off to the layout vendor.